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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/265,819	03/10/1999	MAHITO SHINOHARA	35.C13388	4959

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EXAMINER	
WU, DOROTHY	

ART UNIT	PAPER NUMBER
2615	16

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/265,819	SHINOHARA, MAHITO	
	Examiner	Art Unit	
	Dorothy Wu	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 17-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 17-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 17-22 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sagawa et al, U.S. Patent 3,872,245 in view of the admitted prior art.

Regarding claim 17, Sagawa teaches a sensor chip comprising an image pickup portion (photosensor array) including a plurality of photoelectric conversion elements (photodiodes), which reads on the photoelectric conversion elements (col. 2, lines 46-48); a scan circuit

(sequential pulse generating circuit 100) which reads out a signal from said image pickup portion (photosensor array) (col. 5, lines 10-31; Fig. 6); a reference clock signal generation circuit (clock pulse generating circuit 80) which internally generates a first reference clock signal (Fig. 6); a terminal (node 1 of internal-external changeover circuit 120) which externally inputs a second reference clock signal from outside (col. 5, lines 10-14; Fig. 6); a switch (internal-external changeover circuit 120) connected to at least said reference clock signal generation circuit (clock pulse generating circuit 80) and said terminal, which effects switching between internally driving said image pickup portion and externally driving said image pickup portion (col. 5, lines 10-31; Fig. 6). Sagawa does not teach that the sensor chip is formed on a single semiconductor chip, nor does Sagawa teach a drive pulse generation circuit. The admitted prior art does teach a sensor chip formed on a single semiconductor chip and a drive pulse generation circuit that generates a drive pulse for driving said scan circuit (Fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by Sagawa with the apparatus of the admitted prior art to make a sensor on a semiconductor chip comprising a drive pulse generation circuit, wherein the clock for controlling the scanning operation can be switched between internal and external clocks. One of ordinary skill would have been motivated to make such a modification to achieve more reliable connections and faster operations, as well as use a common driving unit to ensure adequate driving signals for photosensitive elements.

Regarding claim 20, Sagawa teaches a circuit for driving an image pickup portion comprising: a reference clock signal generation circuit (clock pulse generating circuit 80) which internally generates a first reference clock signal (Fig. 6); a terminal (node 1 of internal-external

changeover circuit 120) which externally inputs a second reference clock signal from outside (col. 5, lines 10-14; Fig. 6); and a switch (internal-external changeover circuit 120) connected to at least said reference clock signal generation circuit (clock pulse generating circuit 80) and said terminal, which effects switching between internally driving said image pickup portion and externally driving said image pickup portion (col. 5, lines 10-31; Fig. 6). Sagawa does not teach a drive pulse generation chip formed on a single semiconductor chip that comprises a drive pulse generation circuit which generates a drive pulse. The admitted prior art does teach a drive pulse generation circuit formed on a single semiconductor chip comprising a drive pulse generation circuit which generates a drive pulse (Fig. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by Sagawa with the apparatus of the admitted prior art to make a drive pulse generation chip on a semiconductor chip comprising a drive pulse generation circuit, wherein the clock for controlling the drive pulse generation circuit can be switched between internal and external clocks. One of ordinary skill would have been motivated to make such a modification to achieve more reliable connections and faster operations, as well as use a common driving unit to ensure adequate driving signals for photosensitive elements.

4. Claims 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sagawa et al, U.S. Patent 3,872,245 in view of the admitted prior art, and further in view of Yasuda, U.S. Patent 6,130,710

Regarding claim 18, Sagawa in view of the admitted prior art teach the apparatus of claim 17. See above. Sagawa in view of the admitted prior art do not teach a first control circuit which

effects control so that the drive pulse generation circuit generates the first pulse in a first mode, nor do Sagawa in view of the admitted prior art teach a second mode of operation. Yasuda teaches first and second pulses coming from first and second control circuits (SSG1 **18** and SSG2 **19**) for reading out the signal from said image pickup portion in first and second modes (col. 4, lines 3-9). The admitted prior art teaches a drive pulse generation circuit for driving said scan circuit and a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit (Fig. 1). The terminal that inputs the control signal is inherently taught. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by Yasuda with the apparatus of Sagawa in view of the admitted prior art to make a sensor on a semiconductor chip comprising two sources for reference clock signals for driving the image sensor, one on-chip and one off-chip, with a switch for multiplexing which clock signal will drive the sensor. One of ordinary skill would have been motivated to make such a modification to provide the possibility of driving the sensor in high or low resolution modes.

Regarding claim 19, Yasuda teaches that the first mode is a mode for reading out the signal from said image pickup portion at a resolution lower than that of the second mode (col. 4, lines 3-6).

Regarding claim 21, Sagawa in view of the admitted prior art teach the apparatus of claim 20. See above. Sagawa in view of the admitted prior art do not teach a first control circuit which effects control so that the drive pulse generation circuit generates the first pulse in a first mode, nor do Sagawa in view of the admitted prior art teach a second mode of operation. Yasuda teaches first and second pulses coming from first and second control circuits (SSG1 **18** and

SSG2 **19**) for reading out the signal from said image pickup portion in first and second modes (col. 4, lines 3-9). The admitted prior art teaches a drive pulse generation circuit for driving said scan circuit and a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit (Fig. 1). The terminal that inputs the control signal is inherently taught. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by Yasuda with the apparatus of Sagawa in view of the admitted prior art to make a sensor on a semiconductor chip comprising two sources for reference clock signals for driving the image sensor, one on-chip and one off-chip, with a switch for multiplexing which clock signal will drive the sensor. One of ordinary skill would have been motivated to make such a modification to provide the possibility of driving the sensor in high or low resolution modes.

Regarding claim 22, Sagawa teaches an image pickup apparatus comprising: an image pickup portion (photosensor array) including a plurality of photoelectric conversion elements (photodiodes), which reads on the photoelectric conversion elements (col. 2, lines 46-48); a scan circuit (sequential pulse generating circuit 100) which reads out a signal from said image pickup portion (photosensor array) (col. 5, lines 10-31; Fig. 6); a reference clock signal generation circuit (clock pulse generating circuit 80) which internally generates a first reference clock signal (Fig. 6); a terminal (node 1 of internal-external changeover circuit 120) which externally inputs a second reference clock signal from outside (col. 5, lines 10-14; Fig. 6); a switch (internal-external changeover circuit 120) connected to at least said reference clock signal generation circuit (clock pulse generating circuit 80) and said terminal, which effects switching between internally driving said image pickup portion and externally driving said image pickup

portion (col. 5, lines 10-31; Fig. 6). The first control circuit internal to the apparatus and the second control circuit external to the apparatus are inherently taught.

Sagawa does not teach a sensor chip formed on a single semiconductor substrate or a drive pulse generation circuit which generates a drive pulse for driving said scan circuit. The admitted prior art does teach a sensor chip formed on a single semiconductor chip and a drive pulse generation circuit that generates a drive pulse for driving said scan circuit (Fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the apparatus taught by Sagawa with the apparatus of the admitted prior art to make a sensor on a semiconductor chip comprising a drive pulse generation circuit, wherein the clock for controlling the scanning operation can be switched between internal and external clocks. One of ordinary skill would have been motivated to make such a modification to achieve more reliable connections and faster operations, as well as use a common driving unit to ensure adequate driving signals for photosensitive elements.

Sagawa in view of the admitted prior art do not teach a first control circuit which effects control so that the drive pulse generation circuit generates the first pulse in a first mode, nor do Sagawa in view of the admitted prior art teach a second mode of operation. Yasuda teaches first and second pulses coming from first and second control circuits (SSG1 **18** and SSG2 **19**) for reading out the signal from said image pickup portion in first and second modes (col. 4, lines 3-9). The admitted prior art teaches a drive pulse generation circuit for driving said scan circuit and a control signal from outside said semiconductor chip for controlling said drive pulse generation circuit (Fig. 1). The terminal that inputs the control signal is inherently taught. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

combine the apparatus taught by Yasuda with the apparatus of Sagawa in view of the admitted prior art to make a sensor on a semiconductor chip comprising two sources for reference clock signals for driving the image sensor, one on-chip and one off-chip, with a switch for multiplexing which clock signal will drive the sensor. One of ordinary skill would have been motivated to make such a modification to provide the possibility of driving the sensor in high or low resolution modes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dorothy Wu whose telephone number is 703-305-8412. The examiner can normally be reached on Monday-Friday, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dorothy Wu
DW
June 1, 2004

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